

GI/ITG/GMA Technical Committee "Dependability and Fault Tolerance"

Call for Papers

15thWorkshop on Dependability and Fault Tolerance (VERFE 2019) in conjunction with 32ndARCS 2019, Copenhagen, Denmark, May 20th – 23rd, 2019

Background and Focus Although the basic reliability of hardware and software components has improved over decades, their increasing number causes severe problems. Moreover, in recent years it can be observed that an increasing number of devices are integrated into environments of other physical components such as cars or digital systems. Here, the complexity and number of interactions with these components creates problems with regard to maintaining a dependable operation of the entire system in case of faults or external disturbances. While this is not a problem with microprocessors, shrinking feature sizes, higher complexity, lower voltages, and higher clock frequencies increase the probability of design-, manufacturing-, and operational faults, making fault tolerance techniques in general purpose processors to be of crucial importance in the future. As simple solutions (such as TMR) can easily get too expensive, the ability to trade increased reliability against performance/power overhead will become important, resulting in light-weight fault tolerance techniques implemented in hardware, but controllable from higher software layers.

This workshop aims at presenting contributions and work-in-progress from the research area of dependable and fault-tolerant computing in order to bring together scientists working in related fields.

Topics Contributions on the topic of "Dependable Embedded Systems" are of particular interest; contributions on general topics of dependability and fault tolerance are also welcome but not limited to:

- reliability models for hardware and software
- modeling and simulation of fault-tolerant systems
- fault-tolerant systems and system components
- testing of hardware and software
- failure prediction and fault treatment
- detection and correction of transient faults
- quantitative assessment of reliability improvements
- safety-critical applications
- timeliness problems
- dependability of networks
- dependability of embedded systems
- highly available systems
- dependable organic computing
- self-organization within redundant systems
- dependable ubiquitous and pervasive computing

- composability of dependable systems
- dependable mechatronic systems / micro systems
- · dependability of mobile and wireless systems
- robustness and robustness metrics
- validation and verification
- fault models and fault abstraction
- fault injection techniques
- software-controlled fault tolerance
- on-chip backward recovery techniques (e.g. pipeline flush and re-execution)
- forward recovery techniques (notification of higher layers)
- fault-tolerant caching mechanisms
- dynamic re-use of currently unused resources in processors for fault-tolerance

The workshop will focus on research presentations as well as brainstorming sessions. Therefore, two kinds of contributions are welcome:

- · research papers documenting results of scientific investigations and
- position papers proposing strategies or discussing open problems.

Informations for Authors

Accepted papers will be published by VDE and IEEExplore. Papers should be in English and formatted according to IEEE eXpress "conference mode". Selected papers will appear in the FERS Journal (ISSN **0724-5319**).

Deadlines:

January 25 th , 2019 (extended abstracts (3-4 pages) or full papers, PDF) to:
bernhard.fechner@fernuni-hagen.de
February 11 th , 2019
March 1 st , 2019 (max. 8 pages)
May 20 th or 21 st , 2019

Workshop site: http://arcs2019.itec.kit.edu/downloads/VERFE.pdf

Workshop Chairs

Bernhard Fechner	University of Hagen	Germany
Karl-Erwin Großpietsch	St. Augustin	Germany

Program Committee

Lars Bauer	Karlsruhe Institute of Technology	Germany
Fevzi Belli	University of Paderborn	Germany
Greg Bronevetsky	X - the moonshot factory	USA
Rainer Buchty	TU Braunschweig	Germany
Klaus Echtle	University of Duisburg-Essen	Germany
Wolfgang Ehrenberger	University of Fulda	Germany
Rolf Ernst	TU Braunschweig	Germany
Bernhard Fechner	University of Hagen	Germany
Michael Gössel	University of Potsdam	Germany
Karl-Erwin Großpietsch	St. Augustin	Germany
Jörg Henkel	Karlsruhe Institute of Technology	Germany
John Hursey	Oak Ridge National Laboratory	USA
Jörg Keller	University of Hagen	Germany
Hans-Dieter Kochs	University of Duisburg-Essen	Germany
Minh Lê	Siemens AG Nuremberg	Germany
Miroslaw Malek	USI-Lugano	Switzerland
Erik Maehle	University of Lübeck	Germany
Michael Mock	Fraunhofer IAIS St. Augustin	Germany
Edgar Nett	University of Magdeburg	Germany
Dimitris Nikolos	University of Patras	Greece
Francesca Saglietti	University of Erlangen-Nuremberg	Germany
Toshi Sato	University of Fukuoka	Japan
Martin Schulz	TU Munich	Germany
Muhammad Shafique	TU Vienna	Austria
Peter Sobe	HTW Dresden	Germany
Janusz Sosnowski	University of Warsaw	Poland
Andreas Stopp	Berlin	Germany
Carsten Trinitis	TU Munich	Germany
Peter Tröger	Beuth Hochschule für Technik Berlin	Germany
Heinrich Theodor Vierhaus	TU Cottbus	Germany
Max Walter	Siemens AG Nuremberg	Germany
Norbert Wehn	TU Kaiserslautern	Germany
Josef Weidendorfer	Leibniz Supercomputing Centre/TU Munich	Germany
Sebastian Zug	TU Freiberg	Germany